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Patent

Docket No.: CYPR-CD00232

Information Disclosure Statement Transmittal

I hereby certify that this transmittal of the below described document is being deposited with the United States Postal Service in an envelope bearing First Class Postage and addressed to the Commissioner of Patents and Trademarks, Washington, D.C., 20231, on the below date of deposit.					
Date of Deposit:	02/24/03	Name of Person Making the Deposit:	KATHERINE RINALDI	Signature of the Person Making the Deposit:	Katherine Rinaldi

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Warren Snyder

Serial No.: 10/033,027 Group Art Unit:

Filed: 10/01/01 Examiner:

Title: PROGRAMMABLE SYSTEM ON A CHIP

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Transmittal

Transmitted herewith is the following:

..... Formal drawings, totaling ..... sheets.
..... Informal drawings, totaling ..... sheets.
..... Certification for PTO Consideration
X Information Disclosure statement (3 sheets)
..... Information Disclosure statement and late filing fee
X Form 1449
..... Petition for Extension of Time
X Other: REFERENCES
X Other: Related Pending US Patent Applications

Fee Calculation (for other than a small entity)

Fee Items	Fee Rate	Total
Petition for Extension of Time (fee calculated elsewhere	$ .00	$0.00
Information Disclosure Statement, late filing	$180.00	$0.00
Other:		$0.00
Total Fees		$0.00

PAYMENT OF FEES

1. The full fee due in connection with this communication is provided as follows:

[X] The Commissioner is hereby authorized to charge any additional fees associated with this communication or credit any overpayment to Deposit Account No.: 23-0085 .
A duplicate copy of this authorization is enclosed.

[ ] A check in the amount of $

[ ] Charge any fees required or credit any overpayments associated with this filing to Deposit Account No.: 23-0085.

Please direct all correspondence concerning the above-identified application to the following address:

WAGNER, MURABITO & HAO LLP
Two North Market Street, Third Floor
San Jose, California 95113
(408) 938-9060

Respectfully submitted,

Date: 2/24/2003

By: _____
Anthony C. Murabito
Reg. No. 35,295

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: CYPR-CD00232

Inventor(s): Warren Snyder

Serial No.: 10/033,027 Group Art Unit:

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Title: PROGRAMMABLE SYSTEM ON A CHIP

The Commissioner of Patents and Trademarks
Washington, D.C. 20231
Sir:

Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:

Pat. No.	Pat. Title	Grant Date
6,144,327	PROGRAMMABLY INTERCONNECTED PROGRAMMABLE DEVICES	11/07/00
5,202,687	ANALOG TO DIGITAL CONVERTER	04/13/93
5,880,598	TILE-BASED MODULAR ROUTING RESOURCES FOR HIGH DENSITY PROGRAMMABLE LOGIC DEVICE	03/09/99
6,304,101	PROGRAMMABLE LOGIC DEVICE, INFORMATION PROCESSING SYSTEM, METHOD OF RECONFIGURING PROGRAMMABLE LOGIC DEVICE AND METHOD COMPRESSING CIRCUIT INFORMATION FOR PROGRAMMABLE LOGIC DEVICE	10/16/01
5,426,378	PROGRAMMABLE LOGIC DEVICE WHICH STORES MORE THAN ONE CONFIGURATION AND MEANS FOR SWITCHING CONFIGURATIONS	06/20/95
5,828,693	SPREAD SPECTRUM FREQUENCY HOPPING READER SYSTEM	10/27/98
5,703,871	FACILITATES DATA LINK HANDLER IN A PERFORMANCE MONITORING AND TEST SYSTEM	12/30/97
6,018,559	CHAIN-CONNECTED SHIFT REGISTER AND PROGRAMMABLE LOGIC CIRCUIT WHOSE LOGIC FUNCTION IS CHANGEABLE IN REAL TIME	01/25/00
6,191,660	PROGRAMMABLE OSCILLATOR SCHEME	02/20/01
5,939,949	SELF-ADJUSTING STARTUP CONTROL FOR CHARGE PUMP CURRENT SOURCE IN PHASE LOCED LOOP	08/17/99
6,157,270	PROGRAMMABLE HIGHLY TEMPERATURE AND SUPPLY INDEPENDENT OSCILLATOR	12/05/00
4,138,671	SELECTABLE TRIMMING CIRCUIT FOR USE WITH A DIGITAL TO ANALOG CONVERTER	02/06/79
5,633,766	MAGNETIC DISK STORAGE APPARATUS WITH PHASE SYNC CIRCUIT HAVING CONTROLLABLE RESPONSE CHARACTERISTICS	05/27/97
6,166,367	PROGRAMMABLE ANALOG ARITHMETIC CIRCUIT FOR IMAGING SENSOR	12/26/00
5,600,262	INTEGRATED CIRCUIT FACILITATING SIMULTANEOUS PROGRAMMING OF MULTIPLE ANTIFUSES	02/04/97

5,414,308	HIGH FREQUENCY CLOCK GENERATOR WITH MULTIPLEXER	05/09/95
5,258,760	DIGITALLY DUAL-PROGRAMMABLE NTEGRATOR CIRCUIT	11/02/93
5,563,526	PROGRAMMABLE MIXED-MODE INTEGRATED CIRCUIT ARCHITECTURE	10/08/96
6,225,866	SERIES CONNECTED MULTISTAGE LINEAR FET AMPLIFIER CIRCUIT	05/01/01

The Examiner's attention is respectfully directed to the following Related Pending U.S. Patent Applications:

CYPR-CD00169; "PROGRAMMABLE MICROCONTOLLER ARCHITECTURE (MIXEDANALOG/DIGITAL)"; 08/07/01; 09/924,734; Snyder et al.

CYPR-CD00170; "DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,045; W. Snyder
CYPR-CD00172; "CONFIGURING DIGITAL FUNCTIONS IN A DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,109; W. Snyder

CYPR-CD00173; " A PROGRAMMABLE ANALOG SYSTEM ARCHITECTURE (AS AMENDED)"; 07/18/01; 09/909,047; M. Mar

CYPR-CD00174; "PROGRAMMING METHODOLOGY AND ARCHITECTURE FOR A PROGRAMMABLE ANALOG SYSTEM (AS AMENDED)"; 08/14/01; 09/930,021; Mar et al.

CYPR-CD00175; "METHOD FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE PROGRAMMABLE ANALOG BLOCKS (AS AMENDED)"; 10/01/01; 09/969,311; B. Sullam

CYPR-CD00180; "METHOD AND APPARATUS FOR PROGRAMMING A FLASH MEMORY"; 06/05/01; 09/875;599; W. Snyder

CYPR-CD00182; "IN-SYSTEM CHIP EMULATOR ARCHITECTURE"; 10/10/01; 09/975,115; Snyder et al.

CYPR-CD00187; "A CONFIGURABLE INPUT/OUTPUT INTERFACE FOR A MICROCONTROLLER"; 09/14/01; 09/953,423; Kutz et al.

CYPR-CD00199; "MULTIPLE USE OF MICROCONTROLLER PAD"; 06/26/01; 09/893,050; Kutz et al.

CYPR-CD00226; "PROGRAMMING ARCHITECTURE FOR A PROGRAMMABLE ANALOG SYSTEM"; 08/14/01; 09/929,891; Mar et al.

CYPR-CD00227; "ARCHITECTURE FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE ANALOG PROGRAMMABLE ANALOG BLOCKS"; 10/01/01; 09/969,313; B. Sullam

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Respectfully submitted,

Date: 2/24/2009

By: _____
Anthony C. Murabito
Reg. No. 35,295

Attorney Docket No.: CYPR-CD00232

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Warren Snyder

Serial No.: 10/033,027 Group Art Unit:

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Title: PROGRAMMABLE SYSTEM ON A CHIP

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,144,327	11/07/00	Distinti et al.	341	126	08/12/97
	B	5,202,687	04/13/93	Distinti	341	158	06/12/91
	C	6,166,367	12/26/00	Cho	250	208.1	03/26/99
	D	5,600,262	02/04/97	Kolze	326	38	10/11/95
	E	5,414,308	05/09/95	Lee et al.	327	293	07/29/92
	F	5,258,760	11/02/93	Moody et al.	341	166	07/13/92
	G	5,563,526	10/08/96	Hastings et al.	326	37	01/03/94
	H	6,225,866	05/01/01	Kubota et al.	330	295	06/14/00
	I	5,880,598	03/09/99	Duong	326	41	01/10/97
	J	6,304,101	10/16/01	Nishihara	326	41	06/02/00
	K	5,426,378	06/20/95	Ong	326	39	04/20/94
	L	5,828,693	10/27/98	Mays et al.	375	202	03/21/96
	M	5,703,871	12/30/97	Pope et al.	370	248	05/26/95
	N	6,018,559	01/25/00	Azegami et al.	377	79	12/16/96
	O	6,191,660	02/20/01	Mar et al.	331	111	03/24/99
	P	5,939,949	08/17/99	Olgaard et al.	331	17	03/16/98
	Q	6,157,270	12/05/00	Tso	331	176	12/28/98
	R	4,138,671	02/06/79	Comer et al.	340	347	03/14/77
	S	5,633,766	05/27/97	Hase et al.	360	51	12/21/94

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	T							

Related Pending US Patent Applications

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	U	CYPR-CD00169; "PROGRAMMABLE MICROCONTOLLER ARCHITECTURE (MIXEDANALOG/DIGITAL)"; 08/07/01; 09/924,734; Snyder et al.
	V	CYPR-CD00170; "DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,045; W. Snyder
	W	CYPR-CD00172; "CONFIGURING DIGITAL FUNCTIONS IN A DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,109; Snyder
	X	CYPR-CD00173; " A PROGRAMMABLE ANALOG SYSTEM ARCHITECTURE (AS AMENDED)"; 07/18/01; 09/909,047; M. Mar
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	CC	CYPR-CD00187; "A CONFIGURABLE INPUT/OUTPUT INTERFACE FOR A MICROCONTROLLER"; 09/14/01; 09/953,423; Kutz et al.
	DD	CYPR-CD00199; "MULTIPLE USE OF MICROCONTROLLER PAD"; 06/26/01; 09/893,050; Kutz et al.
	EE	CYPR-CD00226; "PROGRAMMING ARCHITECTURE FOR A PROGRAMMABLE ANALOG SYSTEM"; 08/14/01; 09/929,891; Mar et al.
	FF	CYPR-CD00227; "ARCHITECTURE FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE ANALOG PROGRAMMABLE ANALOG BLOCKS"; 10/01/01; 09/969,313; B. Sullam
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.